Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

What is claimed is:

1. (Currently Amended) A method for sub-sampling pixelized image data gathered in overlapping blocks ~~(B), including the steps of~~comprising:

reading, line by line, from an image memory ~~(M1)~~ containing the pixelized image data;

accumulating as many lines as provided by ~~the~~ a sub-sampling ratio in ~~the~~ a vertical direction, using as many groups of accumulators ~~(Aij)~~ as there are blocks in ~~the~~ a horizontal image direction and as many accumulators per group as provided by the sub-sampling ratio in the horizontal direction; and

memorizing the accumulated values in as many result memories ~~(MR)~~ as there are accumulator groups, each result memory containing sub-sampled matrixes of a number of blocks corresponding to ~~the~~ a number of overlapping blocks in the vertical direction.

2. (Currently Amended) The method of claim 1~~,~~ wherein the memorization is performed in an interlaced fashion.

3. (Currently Amended) The method of claim 1, ~~consisting of~~ further comprising dividing the accumulated values by ~~the~~ a product of the sub-

sampling ratios in both directions, to obtain average values to be memorized as sub-samples.

4. (Currently Amended) The method of claim ~~3,~~ wherein the division of an accumulated value of several lines of the image memory to obtain an average value is obtained by only taking into account a number of most significant bits, smaller than ~~the~~ a number of bits of ~~the~~ a result value.

5. (Currently Amended) The method of claim ~~1,~~ wherein the lines of the image memory ~~(M1)~~ are read successively from ~~the~~ a first one for a number of lines corresponding to the sub-sampling ratio in the vertical direction, after which ~~the~~ a first following line and a previously-used line are alternately read.

6. (Currently Amended) A circuit for sub-sampling pixelized image data distributed in overlapping blocks ~~(B)~~, ~~including~~comprising:

a number of adders ~~(Sij)~~ corresponding to ~~the~~ a number of result block pixels in a first direction, multiplied by ~~the~~ a number of blocks in a second direction;

a number of accumulators ~~(Aij)~~ identical to the number of adders; and

a number of result memories ~~(MR)~~ of ~~the~~ sub-sampled values corresponding to the number of blocks in the first direction.

7. (Currently Amended) The circuit of claim ~~6,~~ wherein the accumulators ~~(Aij)~~ are controllable for addition or subtraction of a current value to ~~the~~ a previously-accumulated result.

8. (Currently Amended) The circuit of claim 6~~,~~ wherein ~~the~~ a number of inputs of each adder corresponds to ~~the~~ a sub-sampling ratio in the first direction.

9. (Currently Amended) The circuit of claim 6~~,~~ wherein said result memories ~~(MR)~~ include a number of lines corresponding to the number of blocks in the second direction, multiplied by the number of pixels of the result blocks in the ~~second~~ first direction.

10. (Currently Amended) The circuit of claim 6~~,~~ wherein ~~the~~ a number of bits of a result value stored in one of said result memories is smaller than ~~the~~ a number of bits of the values of the pixelized image data, ~~the~~ a difference between the two numbers of bits defining ~~the~~ a division ratio for obtaining ~~the~~ an average value of ~~the~~ pixels of each sub-sampled group.

11. (New) An apparatus, comprising:

a first memory to store pixelized image data arranged in overlapping blocks;

a plurality of adders coupled to the memory and having input terminals to receive first values from the first memory that correspond to the stored pixelized image data and to output second values;

a plurality of accumulators respectively coupled to an output terminal of the adders to obtain third values based at least in part on second values output from their respective adders; and

at least one second memory coupled to output terminals of the accumulators to store the third values obtained by the accumulators as domain blocks having a reduced size relative to the overlapping blocks.

12. (New) The apparatus of claim 11 wherein the plurality of adders have a number that corresponds to a number of result block pixels, of the stored pixelized image data, in a first direction, multiplied by a number of blocks of the pixelized image data in a second direction.

13. (New) The apparatus of claim 12, further comprising a plurality of additional second memories, the second memories corresponding in number to a number of blocks in the first direction.

14. (New) The apparatus of claim 11 wherein a number of the accumulators is identical to a number of the adders.

15. (New) The apparatus of claim 11 wherein only certain output terminals of the accumulators provide the third values to the second memory.

16. (New) The apparatus of claim 11 wherein the accumulators are coupled to receive, at one of their input terminals, the third values from their output terminals.

17. (New) The apparatus of claim 11 wherein the accumulators are controllable to add or subtract a current value from a previously obtained value.

18. (New) The apparatus of claim 12 wherein a number of input terminals of each adder to receive the first values from the memory corresponds to a sub-sampling ratio in the first direction.

19. (New) The apparatus of claim 12 wherein the second memory includes a number of lines corresponding to the number of blocks in the second direction, multiplied by a number of result block pixels.

20. (New) The apparatus of claim 11 wherein the third values stored in the second memory include sub-sampled matrices of a number of blocks corresponding to a number of blocks of the pixelized image data in a certain direction.